Title: Low EMI spread spectrum clock oscillators

Background

Traditional ways of dealing with EMI (**E**lectronic **M**agnetic **I**nterference) problems include using EMI filters, ferrite beads, chokes, adding power layer and ground plane to the board, more metal shielding and special coating and RF gaskets. However, the principle sources of EMI problem come from the system clocks including frequency timing generators, crystal oscillators, VCOs and PLLs. It is obvious that the most efficient and economic way to reduce EMI for the whole system is to use low EMI spread spectrum clock (SSC) oscillators. The advantages of using low EMI oscillators are easy passage of regulatory testing, short time-to- market and cost reduction.

Spread Spectrum Technology (SST)

Maximum allowable EMI radiation is normally referred to the peak EMI emissions not the averaged emissions. A good approach is to spread out the concentrated mode energy on one particular frequency to a broader bandwidth and controlled frequency range (for example: center frequency ±1%) with a controlled modulation rate. The total mode energy remains the same but the peak energy got spread out to near-by frequencies. This frequency modulation technique is known as Spread Spectrum Technology (SST). In stead of patching the EMI problems with filtering and shielding, Spread Spectrum Technology (SST) provides efficient and low cost solutions to the expensive EMI problems.

As shown in the following spectrum comparison graphs, a conventional clock (un-modulated) has narrow band width and peak radiation energy. By the SST, a 10 dB or more of the EMI reduction can be expected. The modulation carrier frequency is usually in the range of 6 to 55 KHz (Mercury model and frequency dependent) which makes the modulation process transparent to the oscillator frequency. Consequently, electronic devices have lower EMI emissions but not affected by the resultant instantaneous frequencies.

Center Spread vs Down Spread

The controlled modulation process can be on all of one side of the nominal frequency (**down spread**) or 50% up and 50% down (**center spread**). Pick 100 MHz clock as an example, its center frequency is modulated between 99.500 MHz and 100.500 MHz with center spread of 0.5%; the frequency range is between 99.500 MHz and 100.0 MHz if down spread at 0.5%. By moving the center frequency, a down spread 0.5% modulation can be considered a process equivalent to a center spread of 0.25%. In another word, modulation between 99.500 MHz and 100.0 MHz (down 0.5%) is equivalent to center spread 0.25% with center frequency at 99.750 MHz.

The down spread is preferred if a system can not tolerate operating frequency higher than the nominal frequency (over-clocking problem). Continue to use above 100 MHz clock as example, there is a period of time that the system running between 100.000 MHz and 100.500 MHz, these instantaneous frequencies are higher than the system clock and may erode system timing margin. Using down spread can avoid this problem with the sacrifice of a slightly slower clock rate. **Down-center spread** (also called asymmetric spread), a compromised way of the two, is another choice and available in some Mercury HM series.

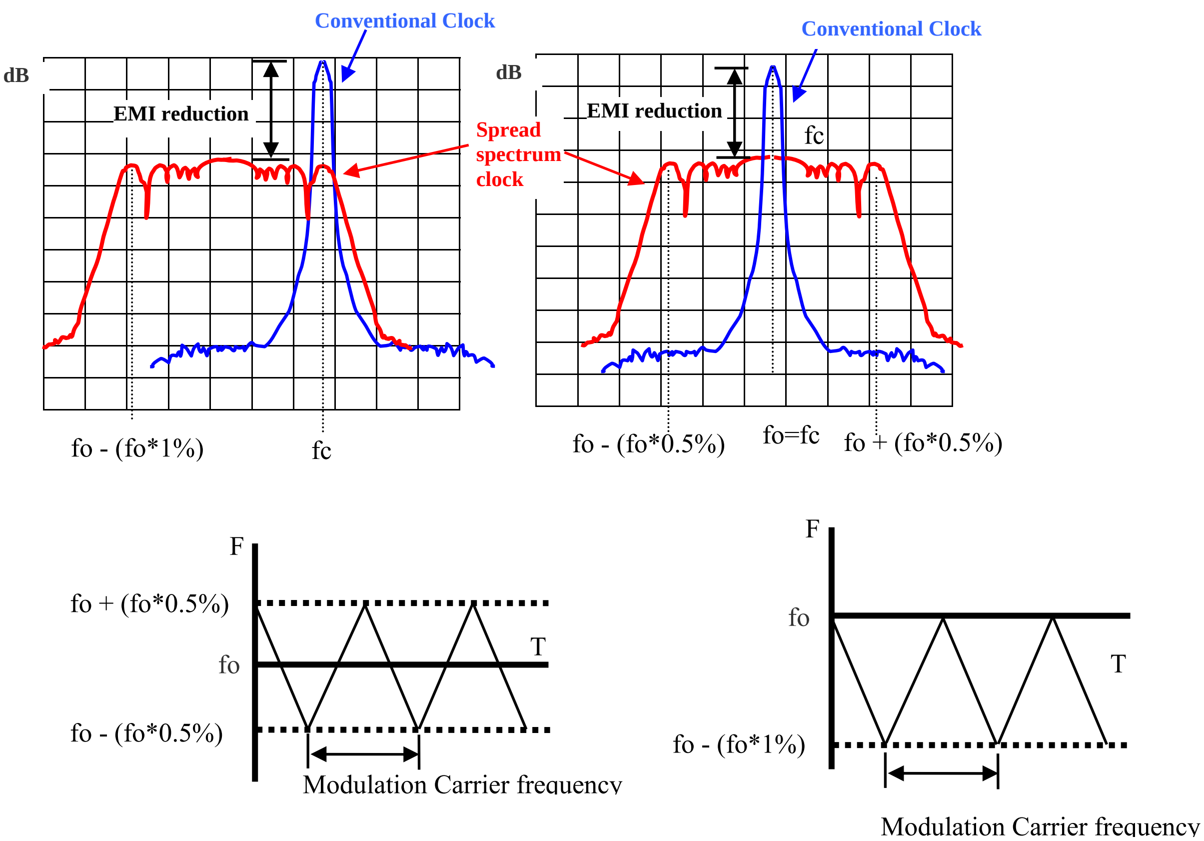


Figure 1: Spectrum comparisons. 1% down spread and ±0.5% center spread as examples

Modulation Carrier Frequency:

The modulation carrier frequency (sweep rate) is typically around KHz range which is relatively slower compared with the MHz range of the clock frequency. As shown in figure 1, the output frequency is slowly swept within the pseudo triangle shape wave envelope from the f(max). to fo(nominal) then to f(min) then to fo(nominal)., back and forth. The resultant instantaneous frequencies are always between f(max) and f(min). The modulation percentage determines the bandwidth of the span while the modulation carrier frequency determines the spacing of the spectral.

EMI Reduction at Harmonics:

As seen in figure 2 and figure 3, higher order harmonic frequencies do get stronger EMI reduction. They also show that the greater modulation percentage reduces EMI emissions more. It needs to be pointed out that the fundamental frequency as well as every harmonics all gets EMI reduction by the SST.

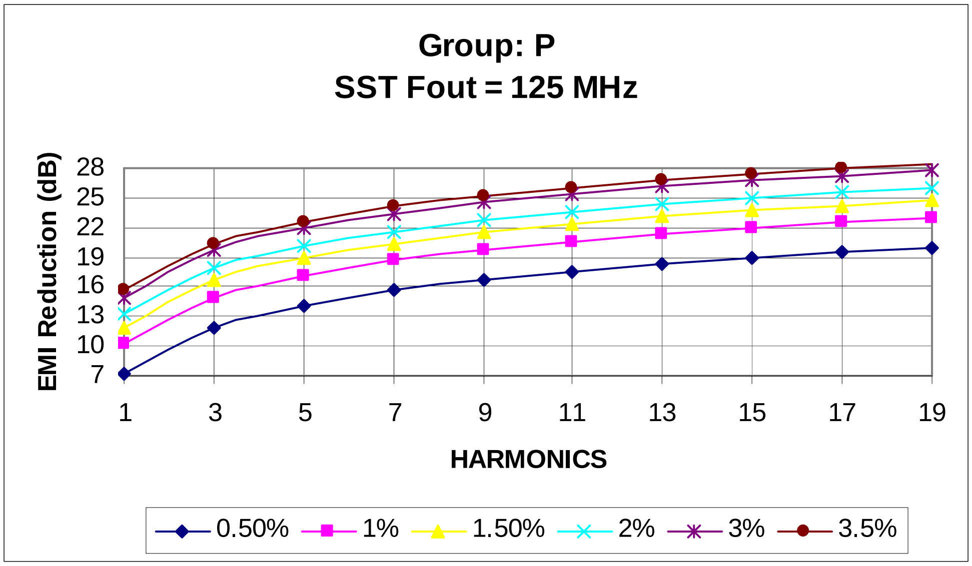


Figure 2: EMI reduction at harmonics for Mercury HM series group **P**

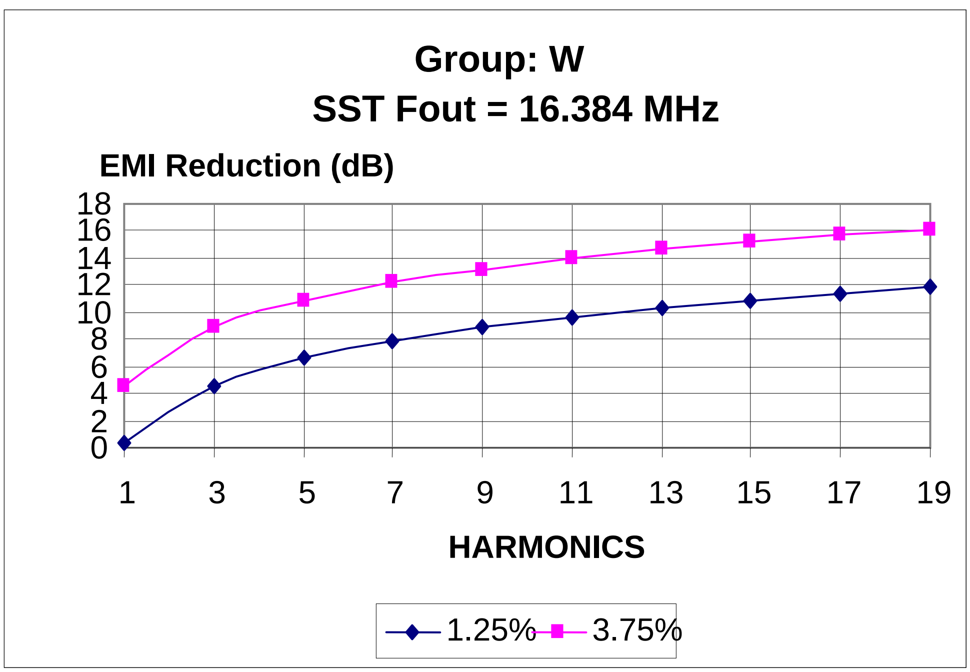
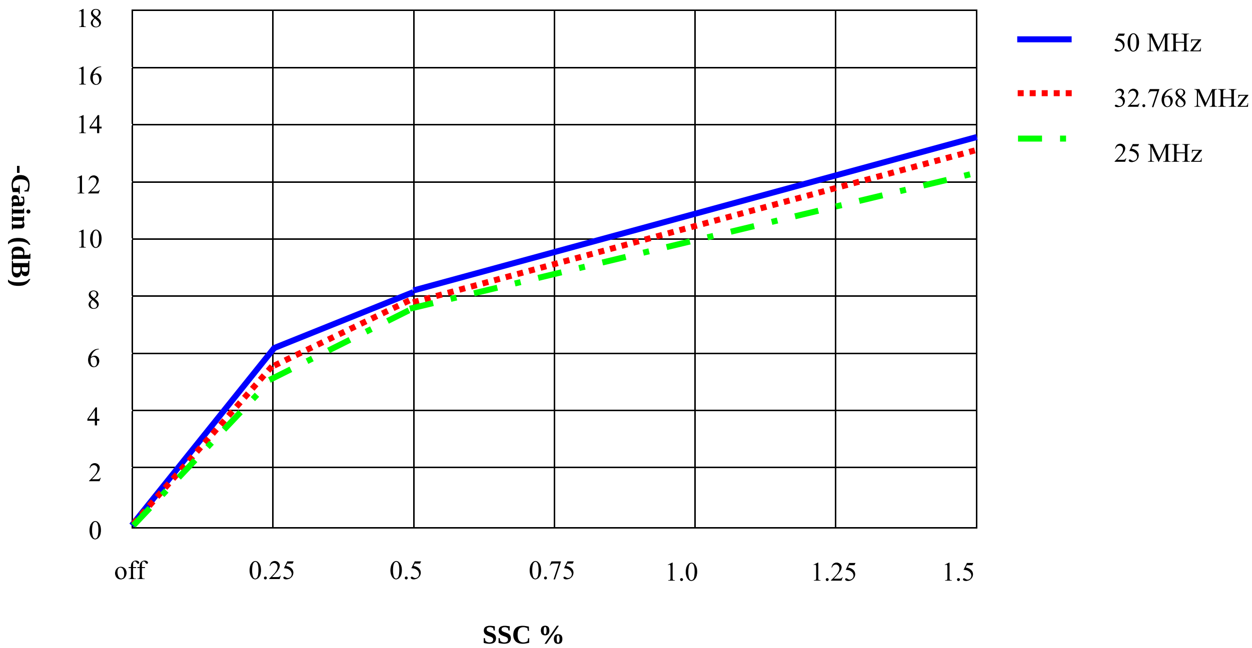


Figure 3: EMI reduction at harmonics for Mercury HM series group **W**

Spectrum Actual Measurement Data:

EMI reduction data shown below are from actual measurement of Mercury 3HM57 series and group "**R**".



	25 MHz	32.768 MHz	50 MHz
SSC is off	-10.1 dB	-9.9 dB	-10.1 dB
SSC=±0.25%	-15.5 dB	-15.6 dB	-16.3 dB
SSC=±0.5%	-17.6 dB	-17.8 dB	-18.2 dB
SSC=±1.5%	-22.3 dB	-23.0 dB	-23.3 dB

Jitter Due to SST Modulation:

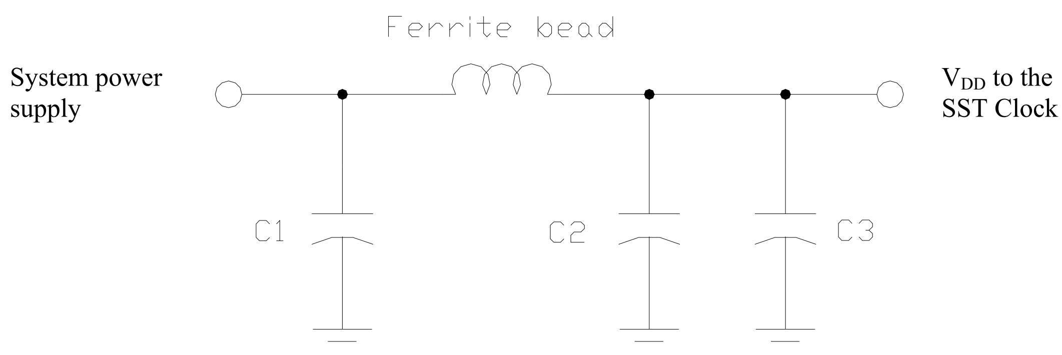
Although the SST modulation is processed in the background and the modulation carrier is at least one thousand times slower compared with the nominal frequency, one still concerns the jitter contributed to the whole system due to the instantaneous frequency. A comparison between clocks with and without SST modulation shows that the modulation process contributes less than 0.05% of the cycle-to-cycle jitter to the system. This negligible jitter contribution makes the spread spectrum oscillators gain more popularity. Mercury 3HM57 series has 250 ps typical and 300 ps max. for the group "R" and ±100 ps max. for the group "P".

When PLL meets SST

Most of the PLLs can work with SST clocks without any timing problem. However, downstream PLLs (defined as PLLs that receive clock signal from other PLLs in the circuit) requires extra precaution in terms of tracking skew. Another area to be concerned is the tracking rate of a PLL needs to be faster than the modulation rate of the SST. All Mercury HM series has modulation carrier frequency below 60 KHz, downstream PLLs with 6 u sec tracking capability will work fine.

Power Supply to the SST Clocks

Power supply filtering plays important role to the EMI reduction and optimum jitter performance. Figure 6 shows the recommended power supply filtering configuration. This lowpass "Π (PI)" filter can remove power supply noise and prevent clock noise from feeding back to the supply. C2, low frequency supply decoupling capacitor, must be a tantalum type and 22 uF is recommended. C3, high frequency supply decoupling capacitor, 0.1 uF ceramic chip capacitor is recommended. C1 can be 0.1 uF ceramic chip capacitor. All capacitors should be placed as close to the SST clock as possible, otherwise the increased trace inductance will negate its decoupling capability.



Series Termination Resistor

If board space allowed and, adding a series resistor of 22 ohms to the SST clock output pin will match the line impedance and thus maintain the signal integrity and further reduce the EMI emissions.